Double-layer Photonic Devices Based on Transfer Printing of Silicon Nanomembranes for Three-dimensional Photonics

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Abstract: We present a novel platform for three dimensional (3D) photonics. A double layer 1x12 multimode interference (MMI) coupler is fabricated using transfer printing of silicon nanomembranes. Optical tests confirm low insertion loss and uniform outputs.
OCIS Codes: (130.3120) Integrated Optics devices; (230.4170) Multilayers

1. Introduction

Vertical integration of multiple layers of active and passive photonic components can resolve the problem of limited real estate on a single layer silicon photonic integrated circuits (PICs) [1]. To date, deposited polysilicon has been used for photonic integration due in part to its applicability in 3D photonic integration [2]. However, the lowest reported propagation loss for polycrystalline silicon waveguides is 6.45dB/cm for rectangular cross-section dimensions of approximately 450 x 250nm [3]. Similar waveguide geometries in crystalline silicon show only ~1dB/cm propagation loss [4]. Additionally, polysilicon process requires high temperature crystallization anneal (~1100˚C), which limits its applications in multilayer active photonic devices with metallic electrodes.

In this paper we demonstrate a novel 3D photonic integration scheme using transfer printing of silicon nanomembranes to serve as top layer device platforms. Transfer printing based assembly techniques represent a potential transformational approach for micro/nanofabrication with far ranging fields of use. At the heart of the method is the use of printing protocols to deposit chemical or physical 'inks' in the precise architectures required by devices [5]. We fabricate double-layer 1x12 MMI couplers, with bottom layer on silicon-on-insulator (SOI) device layer and top layer on transfer printed silicon nanomembrane. MMI couplers can be used for efficient on-chip splitting with optimized design schemes described in [6]. We choose the multimode waveguide width, W_{MMI}=60μm and the corresponding multimode waveguide length, L_{MMI}=553.4μm. The input and output access waveguide width is W_w=2.6μm. At this width, the modal phase errors were greatly reduced. A fanout design is used to increase the separation of each output waveguide to 30μm for resolving the 12 output intensities for near field imaging.

2. Device Fabrication

Figure 1(a) provides a schematic demonstration of the assembly process for double-layer silicon nanomembrane device platform through transfer printing and patterning steps. Device fabrication starts with commercially available SOI from SOITEC with 3μm buried oxide layer (BOX) and 250nm silicon device layer. The fabrication of MMI coupler on the bottom layer using electron beam lithography (EBL) and reactive-ion-etching (RIE) is described in [7]. After etching of the silicon device layer, a 1.5μm thick silicon dioxide layer is deposited using plasma-enhanced chemical vapor deposition (PECVD) as the interlayer dielectric between the bottom and top layer. Next, a thin layer (~500nm) of SU8 epoxy adhesive is spin-cast onto the silicon dioxide surface. Partial curing of the adhesive layer via heating and UV flood exposure provides a flat, firm surface for mounting additional nanomembranes as the top layers.

Silicon nanomembranes derived from a SOI wafer and measuring 2.05mm x 8.05mm x 230nm are released from the hosts by etching in concentrated (49%) HF and retrieved by a bulk piece of PDMS mounted to a rigid glass backing. Figure 1(b) shows a single silicon nanomembrane on the surface of the stamp after retrieval. The inked PDMS is brought in contact with the adhesive-bearing material stack using a custom alignment system with an integrated heating platform. While in contact, the stamp/nanomembrane/substrate system is heated to ~70˚C for 10 minutes to fully cure the adhesive layer. After curing, the stamp is slowly (~500μm/s) retracted from the surface, transferring the aligned silicon nanomembrane to the material stack as the top device layer. Figure 1(c) shows the silicon nanomembrane printed onto the multilayer stack. A silicon dioxide layer of 40nm is deposited using electron beam evaporation as the hard mask for subsequent top layer silicon etching. The MMI coupler on the nanomembrane layer is fabricated using the same EBL and RIE process as the one on the bottom layer.

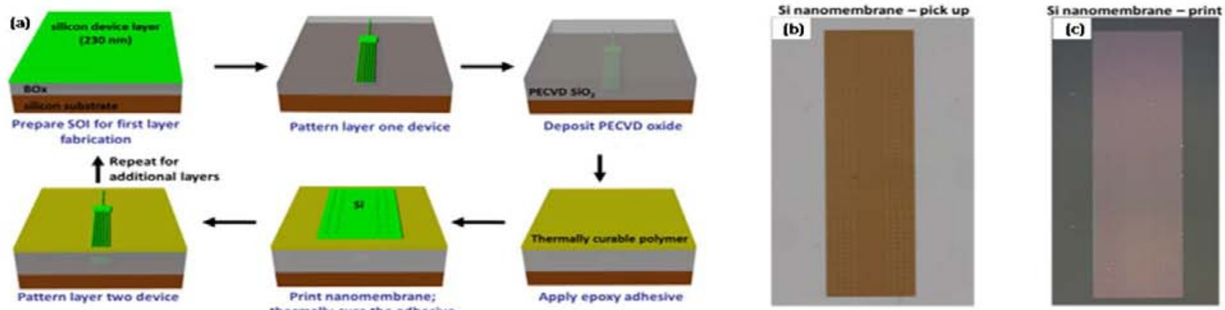

Fig. 1 (a) Schematic process flow for assembling double-layer device on silicon nanomembrane. (b) Silicon nanomembrane on the stamp after retrieval. (c) Silicon nanomembrane on the multilayer stack.

3. Results

Fig 2(a) shows an optical microscope image of the fabricated double-layer MMI coupler while Fig 2(b) provides a SEM view of the cross-section of an output waveguide. An automated aligner system is used to couple Transverse-Electric (TE) polarized light at 1550nm from a polarization maintaining lensed fiber (PMF) with a 2.5µm output mode diameter into the waveguide inputs. An IR CCD camera connected to a variable objective lens captures the top-down near field images of the output waveguides' facets. In order to separate the outputs in the bottom layer from those in the top layer, we etch the output waveguides of the top layer to terminate them before where the bottom layer waveguides end as shown in Figure 2(c). Figure 2(d) shows results of simultaneous excitation of MMI couplers on both layers. Efforts are underway to characterize and optimize the device performance, and also assemble large numbers of stacked silicon nanomembranes and active layers into the device platform.

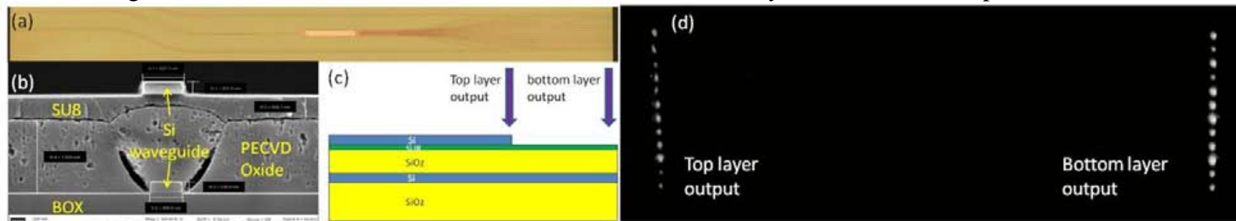

Fig. 2 (a) A microscope picture of the fabricated double-layer MMI coupler. (b) A SEM picture of the cross-section of an output waveguide. (c) A schematic showing separated outputs of bottom and top layers. (d) A top-down IR image of the two 1x12 MMI couplers with simultaneous excitation.

In summary, we present a novel vertical integration scheme of large photonic components on multi layers of low loss crystalline silicon nanomembranes using transfer printing techniques. We developed and demonstrated the patterning and printing processes for assembling double-layer MMI coupler with low insertion loss and uniform outputs, however these processes can be extended to a large number of stacked nanomembrane based photonic devices through repeated patterning and printing. This scheme is a potential solution to the limited silicon real estate for vertical integration of integrated photonic devices, and also serves as platform for novel forms of integrated optical devices.

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