On the fabrication of three-dimensional silicon-on-insulator based optical phased array for agile and large angle laser beam steering systems

Amir Hosseini,[a)] David Kwong, and Yang Zhang
Microelectronic Research Center, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas 78758

Saurabh A. Chandorkar and Filip Crnogorac
Department of Electrical Engineering, Stanford University, Stanford, California 94305

Andrew Carlson
Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

Babak Fallah, Seth Bank, and Emanuel Tutuc
Microelectronic Research Center, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas 78758

John Rogers
Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

R. Fabian W. Pease
Department of Electrical Engineering, Stanford University, Stanford, California 94305

Ray T. Chen[b)]
Microelectronic Research Center, Department of Electrical and Computer Engineering, The University of Texas at Austin, Austin, Texas 78758

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In this article, the authors present and discuss the fabrication of three-dimensional (3D) optical phased array (OPA) devices for large angle, two-dimensional optical beam steering. Fabrication of a single layer (one-dimensional) OPA prototype for one-dimensional beam steering on silicon nanomembrane is presented. The authors present different approaches, such as nanoimprint lithography, optical lithography, and self-aligned patterning of multibonded silicon-on-insulator wafers, for the realization of 3D OPA devices in particular and 3D photonic circuits in general. At the end, the authors discuss the challenges and potential solutions. © *2010 American Vacuum Society.* [DOI: 10.1116/1.3511508]

I. INTRODUCTION

Optical beam steering systems started by mechanical beam directing and stabilization mechanisms, which are subject to limitations such as slow scanning speed (∼kHz). Fast optical phased array (OPA)-based optical beam steering systems were first implemented using nematic liquid crystal cells pioneered by McManamon *et al.*[1] The limitations of these devices, such as limited steering angles ($<5°$), were discussed in detail in Ref. 2. Applications such as free-space laser optical communications in data centers or laser beam scanning radar systems[3] require fast and much larger angle beam steering ($>60°$). We proposed silicon-on-insulator (SOI)-based large steering angle and agile beam steering OPA devices, as shown in Fig. 1.[2] The device consists of a two-dimensional (2D) array of optical waveguides. The phase of the optical signal in each waveguide is actively modulated, so that the output beam is directed in a desired direction through the interference of the output radiations from all the waveguides in the array. The nonuniform array design shown in Fig. 2 enables large angle beam steering while avoiding optical coupling between adjacent waveguides by relaxing the half-wavelength separation requirement. The nonuniform array consists of several subarrays in both directions. Each subarray is a uniform array, but the element spacing differs in different subarrays. The element spacing is such that the main lobes of all the subarrays add up constructively, while there is no overlap between the peak grating lobes of each subarray, resulting in a main lobe and some equiripple side lobes.[2]

Note that each waveguide in the array needs to be single mode. Fabricating the basic waveguides is within the state of the art of current technology. That is, we need to pattern about 300 nm thick single crystal silicon with lines that are 500 nm wide. A waveguide width tolerance of wavelength (in the Si)/50 should be adequate. This comes to about 10 nm so it is just within the capabilities of nanoimprint fabrication techniques and present day optical lithography,[4] respectively, and well within the capabilities of electron beam. The spacing requirements depend on the array design and the tolerance on spacing can be as small as 5 nm, so it could be challenging. However, center line spacing is usually the easi-

[a)]Electronic mail: ahoss@ece.utexas.edu
[b)]Electronic mail: chen@ece.utexas.edu

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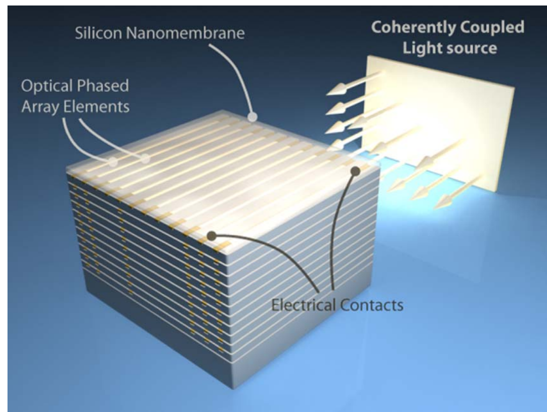

FIG. 1. (Color online)Schematic of silicon nanomembrane-based OPA beam steering.

est dimension to control because it is directly related to the interferometer on the stage of the mask making tool or when using electron beam direct-write of the electron beam tool. The required defect densities should also be reachable. The area of the waveguide array is less than that of current integrated circuits requiring more than 20 levels of patterned structure. Thus, patterning a single layer waveguide array to meet the OPA requirements is within the current state of the art, although more analysis on the effects of dimensional imperfections is needed.

Making a multilevel structure such as that shown in Fig. 2 is a lot more challenging. It is similar to the problems presently being faced by those developing three-dimensional (3D) integrated circuitry in that we need multiple levels of features made in device-quality single crystal silicon or germanium and embedded in SiO_2. It may be necessary to employ some chemical mechanical polishing to ensure sufficiently flat and planar surfaces. The other challenge is the need to accurately align the different layers. If we have only a 10 nm tolerance, then the problem becomes very challenging. Even achieving 100 nm tolerance between levels is only just being approached by some of the groups pursuing 3D integrated circuitry.[5,6]

In this article, we briefly present a fabrication technique of a one-dimensional (1D) OPA and a 12-element OPA device fabricated on a silicon nanomembrane. We also present our theoretical and preliminary fabrication results for multilayer photonics structures. We also discuss the challenges and potential solutions for 3D optical circuitry fabrication.

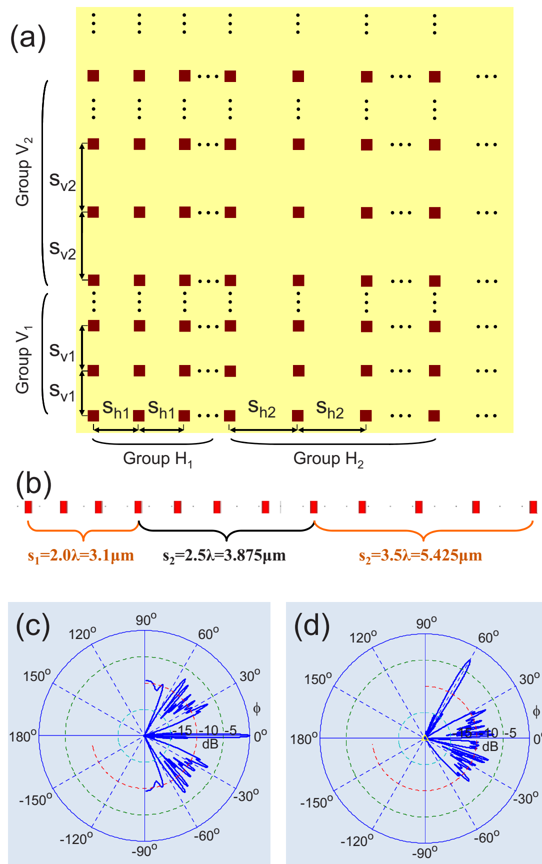

FIG. 2. (Color online) (a) 2D unequally spaced optical phased waveguide array for two-dimensional, large angle optical beam steering. (b) A schematic of the first single layer (1D) unequally spaced optical phased waveguide array prototype with two subgroups and 12 radiating elements. [(c) and (d)] Far-field radiation patterns of the array shown in (b) for the beam at the broad side and steered at 60°, respectively.

II. SINGLE LAYER OPTICAL PHASED ARRAY

In order to demonstrate large angle optical beam steering, we first fabricate a single layer OPA consisting of a 1D OPA of 12 elements, as shown in Fig. 2(b). Beam steering simulation results are shown in Figs. 2(c) and 2(d). The multimode interference couplers (MMIs) were fabricated on commercially available SOI from Soitec with 3 μm buried oxide layer and 250 nm top silicon layer. The silicon was first oxidized to create a 45 nm thick, top oxide layer, which serves as a hard mask for the silicon etch. This oxidation consumes 20 nm of silicon, leaving a final silicon thickness of 230 nm.

The MMIs were patterned using a JEOL JBX6000 electron beam lithography system. A nickel lift-off step was used to invert the pattern, which was subsequently transferred to the top silicon layer via a HBr/Cl_2 based reactive ion etching (RIE). A subsequent piranha clean has the dual purpose of providing a clean sample and, more importantly, removing the nickel etch mask that would cause a large absorption loss from penetration of the electromagnetic tail into the metal layer. Afterward, a 1 μm film of plasma-enhanced chemical vapor deposition (PECVD) silicon dioxide was deposited using the Plasmatherm 790 system for top cladding as well as passivation, and also as a buffer layer between the optical waveguides and the metallic electrodes that provide thermo-optic active phase shifting.

The heater and the wire-bonding pads [see Figs. 3(b) and 3(c)] are 0.15 μm thick Cr/Au films deposited and then patterned using the electron beam lithography system. The electrodes are 1.5 μm wide and 500 μm long to provide 2π

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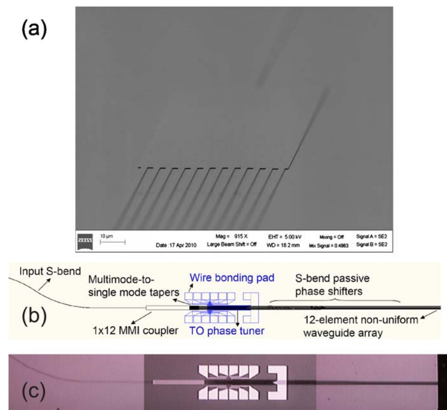

FIG. 3. (Color online) (a) SEM picture of the 1×12 multimode interference beam splitter. (b) A schematic of the 1D OPA device. (c) A microscope image of the fabricated OPA device.

phase and are independently controlled. The far-field characterization and optical beam steering results will be reported separately.

III. FABRICATION TECHNIQUES FOR 3D OPTICAL PHASED ARRAYS

A. Nanomembrane transfer printing

Transfer of semiconductor materials configured in nanoscale geometries (nanomembranes, nanoribbons, and others) can be achieved through the application of rate-dependent printing techniques and a suitable choice of a light interlayer adhesive.[7,8] To affect nanomembrane transfer, following chemical undercut etching schemes designed to release the membrane from the SOI source material, an elastomeric polydimethylsiloxane (PDMS) stamp is brought into conformal contact with the nanomembrane. The stamp is rapidly retracted ($v>1$ cm/s) off the host wafer surface, bringing the nanomembrane with it; the stamp surface can be either a flat, bulk stamp or have molded features of relief such as a line and space grating pattern.[9] Different adhesive layers such as polyimide or photodefinable epoxy (SU8) can also be used to coat the substrate and stamp.[10] After partially curing the adhesive under UV illumination, the PDMS stamp is slowly brought out of contact using micropositioning stages, transferring the nanomembrane to the substrate.

Large area silicon nanomembranes, which serve as waveguiding components in multidimensional OPA after lithographic patterning, have been fabricated from commercially available SOI source materials. SOI wafers (Soitec) having a 260 nm top silicon device layer thickness, 2 μm buried oxide layer, and 400 μm handle layer were coated with a photoactive polymer resist (AZ 5214, 1.5 μm) through spin casting at 3000 rpm for 30 s, followed by a 60 s bake at 110 °C on a hotplate to remove residual solvent. Photolithographic patterning and development of the SOI defined the nanomembrane sheets (rectangles, 500×6000 μm^2). Optimized etch holes 10 μm in diameter, spaced 100 μm in a square packing arrangement, were patterned in the nanomembrane interior for optimized undercut release schemes. Following development, brief RIE (PlasmaTherm) utilizing SF_6 chemistries etched the exposed top layer of silicon. Control of dry etching times and plasma power is critical when fabricating nanomembrane structures to avoid notching effects in the silicon that commonly occur as a result of overexposure to the plasma. The presence of notches in the silicon device layer can lead to crack formation or film fracture during retrieval with a bulk elastomeric stamp.

After plasma etching, the original photoresist mask was removed via sonication in acetone for 3 min and a brief (3 min) piranha solution treatment. The photoresist was reintroduced to the surface using the same conditions as above and patterned to serve as an anchor and reinforcing layer during undercut etch. Wet etching with concentrated HF (49%) removed the buried oxide layer, causing the nanomembrane to sag into light contact with the remaining handle layer of silicon. Figure 4 provides a schematic of nanomembrane fabrication and optical images following dry etching, but prior to undercutting.

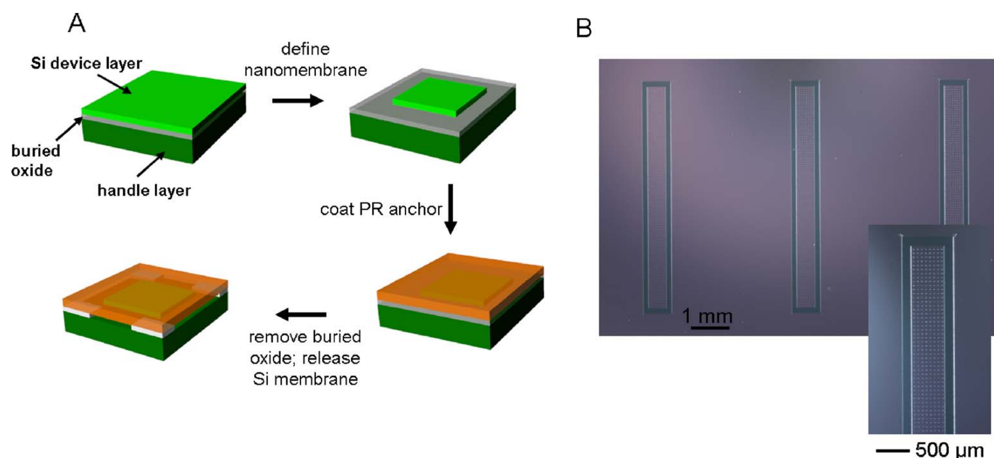

FIG. 4. (Color online) (a) Process flow for silicon nanomembrane fabrication from a SOI source wafer. (b) Nanomembranes after dry etching, but prior to photoresist anchor and HF undercut etching.

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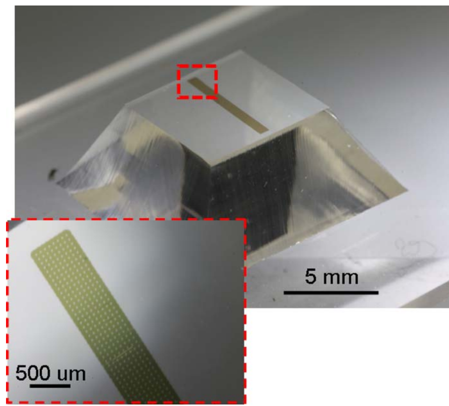

FIG. 5. (Color online) Macroimage of a retrieved nanomembrane ($500 \times 6000\ \mu m^2$) on a bulk PDMS stamp.

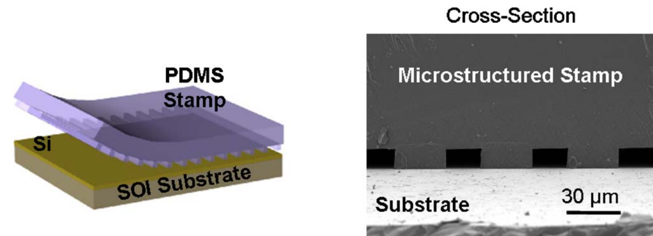

FIG. 6. (Color online) Microstructured stamps used to enhance transfer printing featuring line and space molded surface features (30 μm line width, 20 μm spacing).

Fabricated and released nanomembranes were retrieved from the SOI substrate by bringing a piece of PDMS into conformal contact and rapidly peeling away from the surface. The nonspecific van der Waals interactions between the PDMS elastomer and silicon nanomembrane were sufficient to bond the two together for removal from the substrate with high efficiency. Figure 5 provides optical micrographs of a nanomembrane adhered to a bulk stamp. Contacting the PDMS/Si element to a clear substrate with a light adhesive layer (Norland Optical Adhesive 61, Norland Products), curing under UV illumination, and slowly peeling back the PDMS affected transfer.

Printing efficiency was enhanced through the use of molded relief features on the bulk stamp. In the case of nanomembrane transfer, we introduced a simple line and space grating structure to the surface (30 μm line width, 20 μm spacing), which reduces the contact area between the stamp and silicon, corresponding to a reduction in the adhesive strength of the interface. These stamps were fabricated using well-established casting and curing techniques of soft lithography. A master template was fabricated by patterning via lithography with a photodefinable epoxy (SU-8 25, MircroChem Corp., 25 μm thick), which provided the grating structure. Functionalizing the patterned surface with a vapor deposited trichlorosilane (United Chemical Technology) and thermally curing (70 °C for >2 h) the silicone elastomer polydimethylsiloxane against the template generated the desired stamp surface. A representative illustration and cross section of a microstructured stamp with grating features is shown in Fig. 6.

B. Multilayer nanomembrane stacks for device structures

One of the primary challenges in creating a multilayered OPA is the overlay error between multiple layers after the distortion of a wafer that manifests due to various fabrication steps. For the OPA, the overlay error needs to be on the order of 50–100 nm over a length of 500 μm.

Sequential inking and printing steps following the technique prescribed above can be utilized to fabricate multilayer stacks of nanomembranes, which may prove crucial for flexible manufacturing and rapid prototyping of the systems with the targeted 3D layouts. Figure 7 presents a proposed process flow for the fabrication of complex multilayer stacks designed for OPA devices. Initially, a silicon nanomembrane ($500 \times 6000\ \mu m^2$) is transfer printed onto a target substrate, which will serve as the support structure for the multilayer stacks. Deposition of a SiO_2 dielectric layer (250 nm thick) via PECVD provides the waveguide cladding for the first layer. Next, lift-off photolithographic patterning can be employed to generate metallic thermo-optic heating pads and electrical interconnection points. For this step, the photoresist is patterned to define larger pads along the perimeter of the nanomembrane, which will act as wire-bonding points for external connection. Blanket electron beam evaporation of Ti/Au (1/150 nm; Ti provides adhesion layer) and subsequent rinsing in acetone provide the metallic pads and interconnect lines to the silicon nanomembrane structure. A spin-on dielectric, such as spin-on glass or polyimide, 1.5 μm thick, is then coated onto the silicon/cladding/metal stack to serve as a separation layer and interlayer adhesive. Transfer printing a second silicon nanomembrane and curing the adhesive complete the first level of OPA stack. Anisotropic dry etching of the dielectric using O_2 and CF_4 chemistries defines openings through which to contact the metallic thermal pads.

Additional device layers can be constructed following sequential deposition of dielectric and metal films with lift-off patterning to define contact pads. External connection pads of each fabricated layer should not overlap with the previous layer; a minimum 250 μm offset separation between pads in adjacent layers has been incorporated into these designs. After the completion of multilayer assembly and patterning, electron beam lithography can be used to define waveguides of 500 nm wide and 6 mm long on top of the stack surface. Low molecular weight polymethyl methacrylate acts as both a photopolymer and etch mask during the waveguide formation. After development in a 1:2 solution of methyl isobutyl ketone, anisotropic dry etching can be used to define the waveguide structures throughout the various layers in the OPA stack. Cycles of reactive ion etching with different gas chemistries can be utilized to etch different materials: SF_6 plasma for silicon etching, CF_4 for oxide etching, O_2 for polymer or dielectric etching, and Cl chemistries for gold etching. Following waveguide definition throughout the

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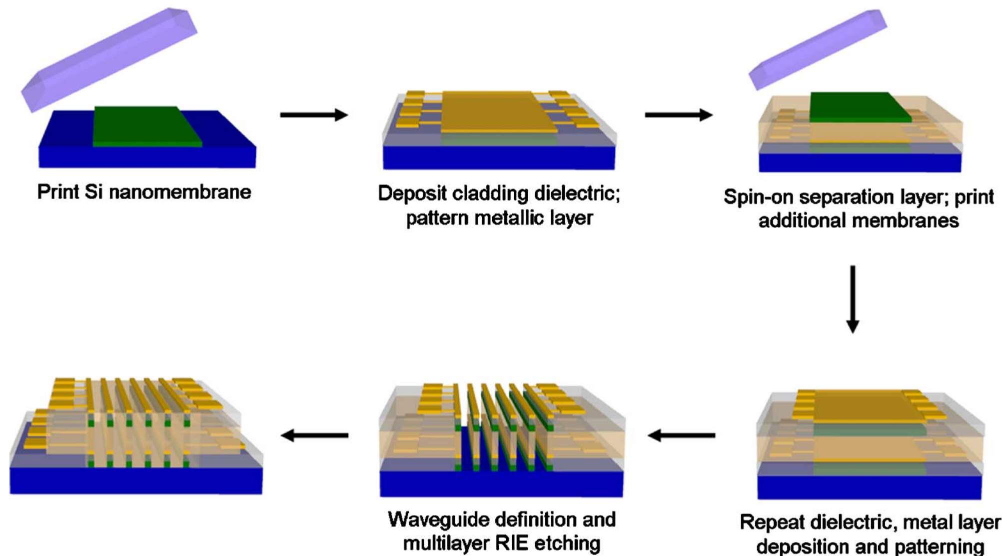

FIG. 7. (Color online) Process flow for generating silicon nanomembrane-based device stacks for multilayer OPA structures. Process shows the fabrication of a two stack device.

stacked structure, PECVD-deposited SiO_2 can used to infill channels between the waveguides, providing structural stability, optimum device isolation, and completion of cladding layers surrounding the waveguide edges. Once the infilling is complete, a final photoresist patterning step and brief dip in concentrated HF allows access to the metallic connection pads, which undergo wire bonding to external electrical control.

The proposed fabrication scheme is advantageous for generating self-aligned waveguides, achieving the sub-20-nm interlayer overlay registration required for high-performance device operation while minimizing potential registration errors that can occur due to the limitations of traditional positioning stages in automated printing tools. Efforts are continuing to fabricate and print these multilayer stacks, configured into device format for phase array functionality.

IV. CHALLENGES AND FUTURE EFFORTS

A. Printer positioning accuracy

To address several of the fabrication and printing challenges posed by the severe alignment requirements of the stacked OPA devices, continuing efforts are focused on quantifying the limits of positioning accuracy of the automated printing tool and identifying nonvisual based alignment protocols during printing. The commercially available linear stages (Aerotech, ALS20000 series) provide rated positioning accuracy and repeatability at ~500 nm. However, linear encoding through control systems can reduce this motion to below the 20 nm positioning requirements for overlay printed stacks. To experimentally test the accuracy of the encoder commands and resulting stage motion, a series of capacitive coupling experiments are being developed, which entails a direct measuring of capacitive change between high-sensitivity probes mounted in the printer toolbit. Two fixed probes (one for each x-, y-direction) provide a reference point for the relative motion of additional probes tethered to the x/y stages. Adjusting the displacement of the probe distance in the $\pm x$, $\pm y$ directions registers as small changes in probe capacitance, which can be measured and, after comparison to a calibration standard, a true distance is extracted. Experiments will chart the actual distance of stage travel compared to commanded distance or position ranging from nanoscale up to micrometer range displacements. Independent confirmation of the travel distance will be obtained through a series of imprinting studies in which ultrasharp (submicrometer curvature) micromachined tips will be indented into a soft polymer or foam surface prior to and after commanded motion. Surface mapping of the substrate via scanning electron microscopy (SEM) or profilometry can measure imprint offset distances.

B. Alignment and overlay of Si nanomembranes

Related to positioning accuracy of the automated transfer printing tool, alignment demand for each printed layer continues to be addressed. Current alignment protocols depend primarily on visual assessment and manual alignment of stages to account for position and tip/tilt accuracy. However, diffraction limited optics limits repeatable accuracy detection to ~2 μm, well above the rated machine motion and waveguide design tolerances. New types of alignment procedures are being investigated for integration into the system. One such area that has attracted attention is through the incorporation of moiré pattern-based fiducial markings onto the substrate or elastomeric stamps. In the simplest embodiment, arrays of fine, nanoscale parallel lines can be patterned onto a receiver substrate prior to printing the first OPA stack layer. A second set of parallel lines having the same geometry, but inclined at a slight angle, can be molded into the stamp used for retrieval and printing of membranes. Proper alignment of the stamp and substrate features generates moiré patterns of

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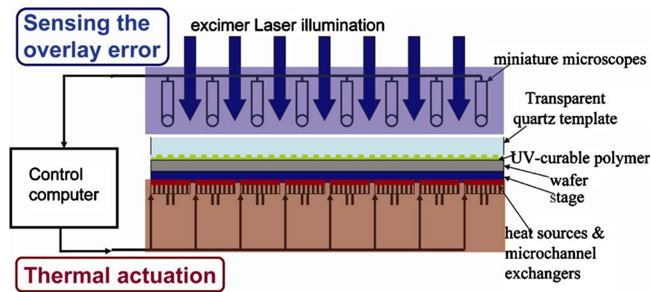

FIG. 8. (Color online) Adaptive nanoimprint system consisting of thermal actuation and sensing subsystems. This approach takes advantage of the transparent nature of a quartz template and the polymer.

alternating visible bands, which can be viewed with the existing optics integrated in the printer tool, indicating alignment of the current nanomembrane with the previous layer. More advanced patterns can be utilized in similar modes for challenging printing steps.

For the more general problem of dealing with distortion due to processing and the overlay error propagated thereby, a novel approach of adaptive nanoimprint lithography can be pursued. In this approach, the wafer is locally heated in an optimal fashion at multiple points to correct for the distortion in real time by obtaining feedback of existing distortion. The real time system achieved by means of microchannel heat sinks using thermal constants as low as 10 ms has been demonstrated.[11] A schematic of this novel approach is depicted in Fig. 8. The number of microscopes needed to accurately estimate the distortion can be determined by finding the bandwidth of the distortion in spatial frequency space. The relative displacement between the wafer and the stamp can be monitored using geometric moiré, which has been shown to achieve resolution as low as 7 nm.[12] The optimal heating of the wafer in order to minimize the overlay error was discussed in Ref. 13 and the results have been summarized in Fig. 9. Asserting the linearity of the heat equation, one can consider each heater's effect separately and record the displacement $(\alpha(x,y), \beta(x,y))$ arising from thermal expansion in the area of interest. The optimal heat inputs q_i can be obtained by solving the convex optimization problem [Fig. 9(a)]:

$$\min[\text{squared error}] = \min\left[\int_{\text{area of interest}} \left(X(x,y) + \sum_i \alpha_i q_i\right)^2 + \left(Y(x,y) + \sum_i \beta_i q_i\right)^2 dxdy\right] \quad \text{subject to} \quad q_{i\text{-heaters}} > 0.$$

Figure 9(b) summarizes the thermal and mechanical boundary conditions used to solve the above optimization problem in the finite element method (FEM) simulations. Figure 9(c) depicts an example of correction of an overlay error in the form of second harmonic shear strain. As the result of the strain, the rms displacement in the area of interest is 27 nm and is reduced to 9 nm by optimal heating of the wafer.

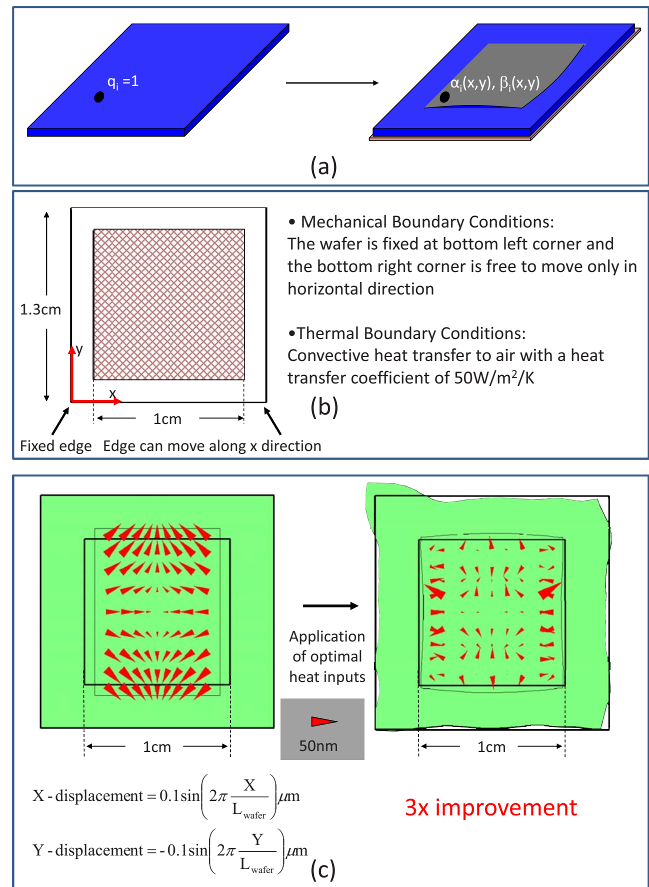

FIG. 9. (Color online) FEM simulation results for optimal heat inputs at various localized regions on the wafer show that substantial improvement in overlay error can be achieved even in the case of shear strain. (a) The optimal heat inputs are obtained by solving a constrained convex optimization problem. (b) The boundary conditions used in the FEM simulation. [c] Various cases of simulated strain and the reduction achieved after application of the optimal heat inputs.

Note that the output phase values can be electronically corrected. However, poor layer-to-layer alignment results in large "static" power consumption. In this case, even when the optical beam is not steering in any direction, a large power is consumed for phase correction; otherwise, large side-lobe-levels would result in extremely poor diffraction efficiency (the ratio of the power directed in the desired direction to the power directed in all directions). Therefore, although an electronic phase correction can be used to partially relax the layer-to-layer alignment requirement, it will not be an option to fix large errors for low-power optical phased arrays, which are our targets.

C. Multilayer self-aligned waveguides

The process flow for waveguide self-alignment is advantageous for relaxing the overlay requirements for printing nanomembranes onto layers that have already undergone extensive fabrication and waveguide definition. However, significant engineering challenges are presented in the fabrication and etching through an as-stacked structure, as shown in the penultimate panel of Fig. 7. The most challenging of

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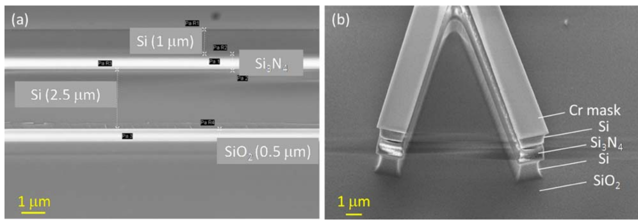

FIG. 10. (Color online) (a) Cross sectional SEM or a double bonded SOI wafer. The top dielectric is a Si_3N_4 layer, while the second is SiO_2. (b) Cross sectional SEM of a splitter realized using double bonded SOI wafers.

these obstacles is expected to be the optimized etching cycles to define waveguides through all the assembled layers. Etching will create mechanically fragile structures that may not be robust to the necessary patterning and masking steps required to protect other layers of the system. Appropriate mask materials and strategies must also be developed so as to protect top device layers from continuous exposure to the different plasma etching conditions. Additionally, interlayer materials must be optimally matched for thermal and optical properties to minimize stress buildup during high temperature processing (PECVD) and ensure good waveguiding properties. Figure 10 shows the results of preliminary efforts to create self-aligned waveguides. We already have the capability of bonding single crystal silicon to create the multiple device layers.[14] Starting from a multibonded SOI, which has silicon, silicon nitride, or silicon dioxide layers of appropriate thicknesses [Fig. 10(a)], vertically aligned waveguides are fabricated through multiple cycles of etching [Fig. 10(b)]. We have observed undercutting, especially in the silicon layers. We also noticed different waveguiding cross-section profiles in different layers. Design work and initial fabrication steps are underway to investigate and address these issues.

V. SUMMARY

In this article, we presented and discussed the fabrication of 3D OPA devices for large angle optical beam steering. Fabrication of a single layer OPA device was presented. Potential approaches to full 3D OPA devices and our recent progress were discussed. In the end, we reviewed the challenges and potential solutions to the realization of 3D OPA devices.

ACKNOWLEDGMENTS

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