

## On-chip intra- and inter-layer grating couplers for three-dimensional integration of silicon photonics

Yang Zhang, David Kwong, Xiaochuan Xu, Amir Hosseini, Sang Y. Yang et al.

Citation: *Appl. Phys. Lett.* **102**, 211109 (2013); doi: 10.1063/1.4808208

View online: <http://dx.doi.org/10.1063/1.4808208>

View Table of Contents: <http://apl.aip.org/resource/1/APPLAB/v102/i21>

Published by the [American Institute of Physics](http://www.aip.org).

---

### Additional information on *Appl. Phys. Lett.*

Journal Homepage: <http://apl.aip.org/>

Journal Information: [http://apl.aip.org/about/about\\_the\\_journal](http://apl.aip.org/about/about_the_journal)

Top downloads: [http://apl.aip.org/features/most\\_downloaded](http://apl.aip.org/features/most_downloaded)

Information for Authors: <http://apl.aip.org/authors>

## ADVERTISEMENT



Improve your Images with Minus K's  
**Negative-Stiffness** Vibration Isolation

Workstations & Optical Tables



Custom Applications



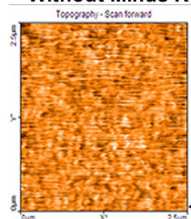
Bench Top Isolators



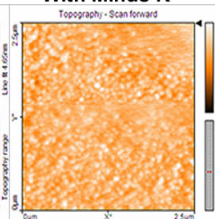
Multi Isolator Systems



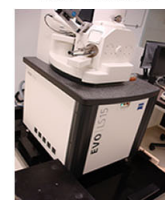
Without Minus K



With Minus K



Floor Platforms



## On-chip intra- and inter-layer grating couplers for three-dimensional integration of silicon photonics

Yang Zhang,<sup>1,a)</sup> David Kwong,<sup>1</sup> Xiaochuan Xu,<sup>1</sup> Amir Hosseini,<sup>2</sup> Sang Y. Yang,<sup>3</sup> John A. Rogers,<sup>3</sup> and Ray T. Chen<sup>1,a)</sup>

<sup>1</sup>Microelectronic Research Center, Department of Electrical and Computer Engineering, The University of Texas, 10100 Burnet Rd., Austin, Texas 78758, USA

<sup>2</sup>Omega Optics, Inc., 10306 Sausalito Dr., Austin, Texas 78759, USA

<sup>3</sup>Department of Materials Science and Engineering, Beckman Institute, and Frederick Seitz Materials Research Laboratory, University of Illinois at Urbana-Champaign, Illinois 61801, USA

(Received 21 January 2013; accepted 13 May 2013; published online 30 May 2013)

We present on-chip intra- and inter-layer grating couplers fabricated on double-layer, single crystalline silicon nanomembranes. The silicon nanomembranes were fabricated using an adhesive bonding process. The grating couplers are based on subwavelength nanostructures operating at the transverse-electric polarization. Such nanostructures can be patterned in a single lithography/etching process. Simultaneous intra-layer coupling to separate silicon photonic layers is demonstrated through grating couplers with peak efficiencies of 18% and 44% per grating coupler for bottom and top layer, respectively, at 1550 nm wavelength. The inter-layer grating coupler has an efficiency of 25% at 1560 nm wavelength with a 3 dB bandwidth of 41 nm. © 2013 AIP Publishing LLC.

[<http://dx.doi.org/10.1063/1.4808208>]

Silicon photonics is considered a promising solution for on-chip low power and high bandwidth interconnects.<sup>1</sup> To date, most silicon photonic devices and circuits are demonstrated on the silicon-on-insulator (SOI) platform.<sup>2,3</sup> However, considering the minimum spacing between optical waveguides to avoid crosstalk and the relatively large sizes of on-chip photonic components, such as low-loss waveguide crossings and beam splitters,<sup>4,5</sup> the bandwidth density (Gbs/ $\mu\text{m}$ ) of single-layer silicon photonic chips is limited.<sup>6</sup> Vertical integration of multiple layers of photonic components can ameliorate the limited bandwidth density on a single layer photonic integrated circuit (PIC).<sup>7</sup> Double-layer silicon PICs have been demonstrated with film deposition approaches, including hydrogenated amorphous silicon and polycrystalline silicon.<sup>8,9</sup> On-chip inter-layer grating coupling was accomplished with amorphous silicon layers,<sup>10</sup> but amorphous silicon has a very low charge mobility, which limits its application in high-speed PICs. Single crystalline silicon is the most desirable material for multi-layer silicon PICs due to its superior material properties such as low material absorption loss and high carrier mobility. Unlike amorphous silicon and polycrystalline silicon, single crystalline silicon layers cannot be realized by deposition. Other approaches have been investigated to build double-layer structures comprised of crystalline silicon, including silicon nanomembrane transfer<sup>11,12</sup> and direct wafer bonding.<sup>13</sup> However, coupling between separate layers has not been demonstrated in the aforementioned methods. Adhesive bonding, which has been used in fabricating photonic devices on single crystalline silicon nanomembrane,<sup>14,15</sup> serves as a good candidate for fabricating double-layer PICs.

Various grating couplers have achieved coupling between photonic layers.<sup>16–18</sup> However, these are only

suitable for inter-chip applications, and the grating couplers are based on partially etching of silicon layers, which require additional lithography and etching steps to define waveguides. Subwavelength nanostructure based grating couplers can be patterned and etched in the same step with the silicon waveguide layer and thus simplify the fabrication process comparing to partially etched grating couplers. Subwavelength nanostructures provide high coupling efficiency with large optical bandwidth while providing anti-reflection mechanism through destructive interference in intra-layer grating coupler applications on SOI wafers and adhesively bonded silicon nanomembranes.<sup>19,20</sup>

In this paper, we present vertically integrated, double-layer, on-chip, single crystalline silicon nanomembranes as a platform for 3D photonic integration. We demonstrated simultaneous coupling to both silicon layers through intra-layer grating couplers based on subwavelength nanostructures and inter-layer coupling between silicon layers through a subwavelength nanostructure based inter-layer grating coupler.

Figure 1 shows a 3D schematic of our intra- and inter-layer grating couplers. Light is coupled from a polarization maintaining fiber (PMF) with a core diameter of  $9\ \mu\text{m}$  to an area-matched linearly tapered waveguide, followed by a  $2.5\ \mu\text{m}$  wide waveguide on the bottom layer through grating 1, and then coupled to a  $2.5\ \mu\text{m}$  wide waveguide on the top layer through inter-layer grating coupler, which consists of grating 2 and grating 3. The light is then coupled out to a single mode fiber (SMF) with a core diameter of  $9\ \mu\text{m}$  through grating 4. The grating regions are connected to  $2.5\ \mu\text{m}$  wide waveguides using  $500\ \mu\text{m}$  long linear tapers. The two silicon nanomembranes on different layers are  $0.25\ \mu\text{m}$  thick with refractive indices of 3.47. The Buried Oxide (BOX) layer has a thickness of  $3\ \mu\text{m}$  and a refractive index of 1.45. The gratings on both layers are formed by periodically patterning parts of silicon layer into subwavelength nanostructures,

<sup>a)</sup> Authors to whom correspondence should be addressed. Electronic addresses: yangzhang@utexas.edu and raychen@uts.cc.utexas.edu.

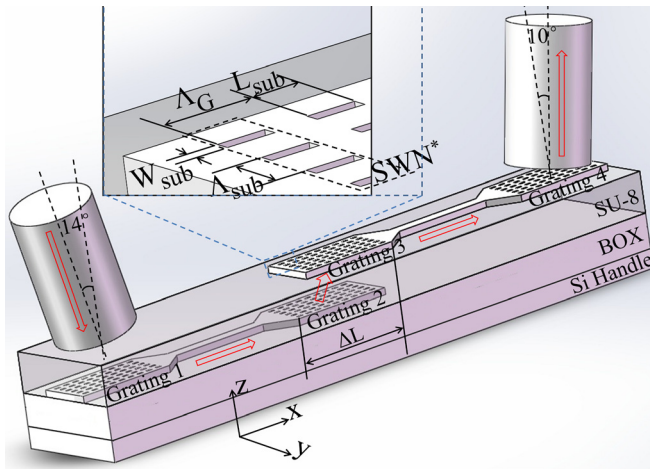


FIG. 1. A 3D schematic of the intra- and inter-layer grating couplers (SWN denotes subwavelength nanostructure).

whose refractive indices can be engineered to accommodate grating coupler design.

The design of subwavelength nanostructure follows the method described in Refs. 19 and 20. Figure 1 shows a schematic of 1D stratified subwavelength nanostructure used in our grating couplers. Silicon and etched rectangular holes are periodically laminated to form the subwavelength nanostructure.  $\Lambda_{\text{sub}}$  is the period of subwavelength nanostructure,  $W_{\text{sub}}$  is the width of the rectangular etched hole, and  $L_{\text{sub}}$  is the length of the rectangular etched hole. The refractive index of the subwavelength nanostructure ( $n_{\text{sub}}$ ) is a function of  $\Lambda_{\text{sub}}$ ,  $W_{\text{sub}}$ , operating wavelength ( $\lambda$ ), and the refractive index of the material in the etched holes ( $n_{\text{hole}}$ )<sup>21</sup> and can be engineered by tuning  $W_{\text{sub}}$  with a fixed  $\Lambda_{\text{sub}}$ . The gratings based on subwavelength nanostructure are treated as conventional grating couplers in the inter-layer grating coupler design described below.

The inter-layer grating coupler consists of grating 2 and grating 3. We used 25 periods and 50% grating duty cycle ( $L_{\text{sub}} = \Lambda_G/2$ ) for both grating 2 and grating 3. Grating period ( $\Lambda_G$ ), grating 2's subwavelength nanostructure's refractive index ( $n_{\text{sub}1}$ ), grating 3's subwavelength nanostructure's refractive index ( $n_{\text{sub}2}$ ), SU-8 layer thickness ( $t_{\text{SU-8}}$ ), and effective length ( $\Delta L$ ), which is defined as the distance between the start of grating 2 and the end of grating 3, were optimized by 2D finite-difference-time-domain (FDTD) simulations. The input light is assumed to be Transverse-Electric (TE) polarized at 1550 nm operating wavelength. We found that the maximum coupling efficiency of the inter-layer grating coupler is 21% with  $\Lambda_G = 820$  nm for both grating 2 and grating 3,  $n_{\text{sub}1} = 2.5$ ,  $n_{\text{sub}2} = 2.55$ ,  $t_{\text{SU-8}} = 3.7 \mu\text{m}$ , and  $\Delta L = 12.0 \mu\text{m}$ . We used  $\Lambda_{\text{sub}} = 390$  nm for the subwavelength nanostructures of both grating 2 and grating 3.  $W_{\text{sub}}$  of grating 2 was calculated to be 141 nm with  $n_{\text{hole}} = 1.575$  and  $n_{\text{sub}} = 2.5$ .  $W_{\text{sub}}$  of grating 3 was calculated to be 70 nm with  $n_{\text{hole}} = 1$ ,  $n_{\text{sub}} = 2.55$ .<sup>19</sup>

Figure 2 shows the electric field distribution calculated by 2D FDTD simulations with the optimized structural parameters. Light is coupled from the waveguide on the bottom layer to the waveguide on the top layer through the inter-layer grating coupler. Different colors represent the intensity

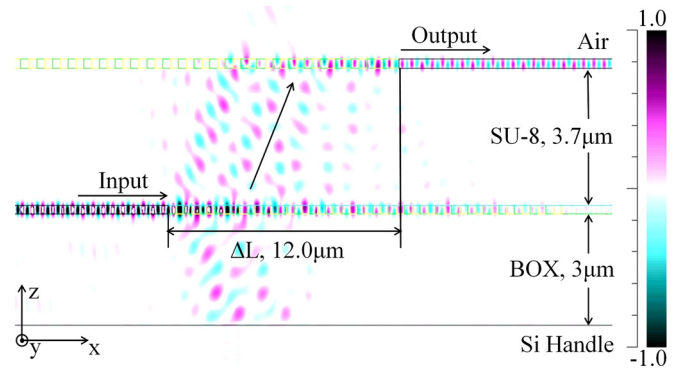


FIG. 2. The electrical field distribution of the optimized inter-layer grating coupler calculated using 2D FDTD.

of the electric field. Note that the power upward emitting angle of grating 2 and the power downward emitting angle of grating 3 are both  $22^\circ$  in our design at 1550 nm operating wavelength.

Grating 1 and grating 4 were optimized using a 2D simulation package CAMFR based on eigenmode expansion. We used 50% grating duty cycle for both grating 1 and grating 4. An exhaustive parameter sweep of their  $\Lambda_G$  and  $n_{\text{sub}}$  combinations show that their maximum power upward efficiencies are 26% and 59% for grating 1 and grating 4, respectively, with the parameters shown in Table I. The power upward emitting angles for grating 1 and grating 4 are  $14^\circ$  and  $10^\circ$ , respectively. The size of grating 4 was chosen to match the mode size of a SMF.<sup>19</sup> The width of grating 1 was chosen to be larger than that of grating 4 to account for the field divergence induced by light propagating in the SU-8 layer on top of grating 1, as well as to increase the fiber-to-chip alignment tolerance. Giving  $\Lambda_{\text{sub}} = 390$  nm for both gratings, grating 1 has a  $W_{\text{sub}}$  of 202 nm, which corresponds to  $n_{\text{sub}}$  of 2.15, and grating 4 has a  $W_{\text{sub}}$  of 80 nm, which corresponds to  $n_{\text{sub}}$  of 2.45. The parameters of grating 1, 2, 3, and 4 are summarized in Table I. For grating 2 and grating 3, their lengths were given by aforementioned simulations. Grating 3 was designed to be wider than grating 2 to compensate for the field divergence as light propagates in the SU-8 layer, as well as to increase the alignment tolerance between two layers in y-direction (as defined in Figure 1).

The fabrication process flow of the devices is illustrated in Figure 3. Gratings on the bottom layer were fabricated on an SOI chip (250 nm single crystalline silicon device layer and  $3 \mu\text{m}$  BOX layer) using Electron Beam Lithography (EBL) and Reactive Ion Etching (RIE). This SOI chip served as recipient substrate in adhesive bonding process. Another SOI chip was used as donor substrate in adhesive bonding

TABLE I. The parameters of grating 1, 2, 3, and 4.

	No. of Length ( $\mu\text{m}$ )	No. of Width ( $\mu\text{m}$ )	No. of grating period	$\Lambda_G$ (nm)	No. of subwavelength period	Duty cycle (%)	$\Lambda_{\text{sub}}$ (nm)	$W_{\text{sub}}$ (nm)	$n_{\text{sub}}$
Grating 1	17	13	23	735	32	50	390	202	2.15
Grating 2	20.5	10	25	820	26	50	390	141	2.5
Grating 3	20.5	13	25	820	32	50	390	70	2.55
Grating 4	17	10	25	690	26	50	390	80	2.45

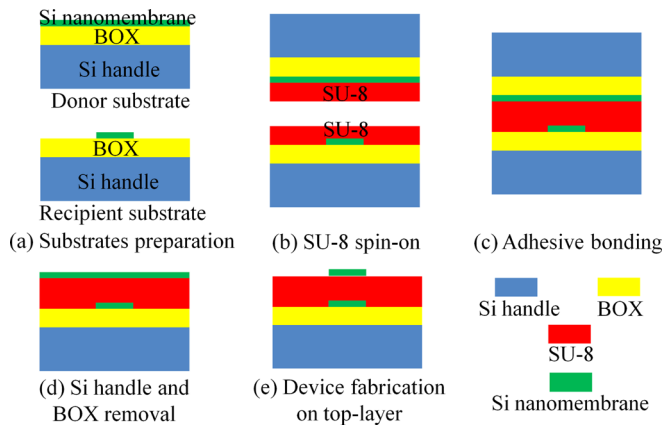


FIG. 3. A schematic of the fabrication process flow. (a) Substrates preparation. (b) Spinning-on SU-8 onto substrates. (c) Adhesive bonding. (d) Si handle and BOX removal. (e) Device fabrication on top-layer.

process (Figure 3(a)).  $\sim 2\ \mu\text{m}$  thick SU-8 layers were spun onto both the recipient and donor substrates, followed by a 2 min pre-bake at  $95^\circ\text{C}$  to evaporate the solvent (Figure 3(b)). SU-8 has excellent self-planarization characteristics and low optical loss<sup>22</sup> at the optical communication wavelength range, which makes it an ideal adhesive material in our fabrication process. Next, the two substrates were brought in close contact using a home-made chip bonder, which uniformly applied pressure, and kept in a  $90^\circ\text{C}$  oven to ensure sufficient reflow of SU-8 for trapped air bubble removal to give high quality bond (Figure 3(c)). After adhesive bonding, the silicon handle of the donor substrate was first polished down to  $\sim 100\ \mu\text{m}$  thick and then removed by Deep Reactive Ion Etching (DRIE). The BOX layer of the donor substrate served as an etch-stop layer in the DRIE process and also protected the device layer of the donor substrate before future process. After the silicon handle was removed, the SU-8 layer was exposed to ultraviolet (UV) irradiation

through the donor substrate and post-baked for UV induced polymer crosslinking and hardening. The BOX layer of the donor substrate was then removed by wet etching in 49% hydrofluoric acid (Figure 3(d)). Finally, gratings were fabricated on the top layer using EBL and RIE (Figure 3(e)).

A cross-sectional Scanning Electron Microscopy (SEM) image of the bonded double-layer silicon nanomembranes is shown in Figure 4(a). A SEM image of the fabricated grating 2 on the bottom layer before adhesive bonding is shown in Figure 4(b). Note that the rectangular etched holes on the bottom layer were filled with SU-8 during the bonding process, as shown in Figure 4(c). The alignment between two silicon PICs on the top and bottom silicon nanomembranes within 100 nm accuracy was realized by electron beam scanning of gold alignmarks on the bottom silicon nanomembrane.

The testing setup is shown in Figure 1. Input light is from a broad band amplified spontaneous emission (ASE) source with TE polarization. The input and output fiber tilting angles were adjusted to be  $14^\circ$  and  $10^\circ$  from normal incidence, respectively. The measured fiber-to-fiber coupling efficiency normalized to the light source is shown in Figure 5(a). In order to extract the coupling efficiency of the inter-layer grating coupler, it is necessary to measure the coupling efficiency of grating 1 and grating 4 first.

The testing setup to measure grating 1 and grating 4 is described in Refs. 19 and 20. The peak efficiencies for grating 1 and grating 4 were measured to be 18% ( $-7.4\ \text{dB}$ ) and 44% ( $-3.6\ \text{dB}$ ), respectively, as shown in Figures 5(b) and 5(c). Taking into account the mismatch between the electric field distributions of power upward and optical fiber, the measured coupling efficiencies agree well with the simulated values.

Assuming negligible loss for linear tapers and connecting waveguides, we extracted the coupling efficiency of the inter-layer grating coupler by subtracting the coupling efficiencies of grating 1 and grating 4 from the coupling

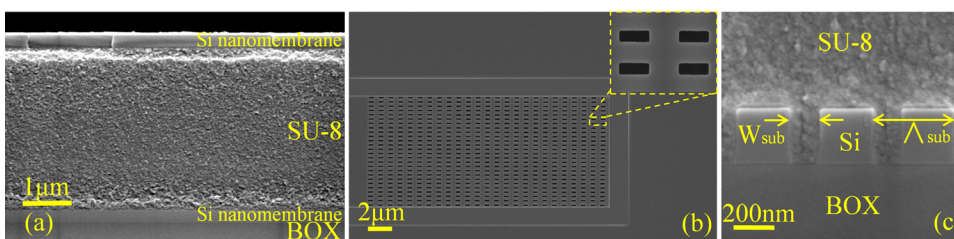


FIG. 4. (a) A cross-sectional SEM image of the fabricated double-layer silicon nanomembranes. (b) A SEM image of the fabricated grating 2 before adhesive bonding. (c) A cross-sectional SEM image of the subwavelength nanostructure on the bottom layer showing SU-8 filling the etched holes.

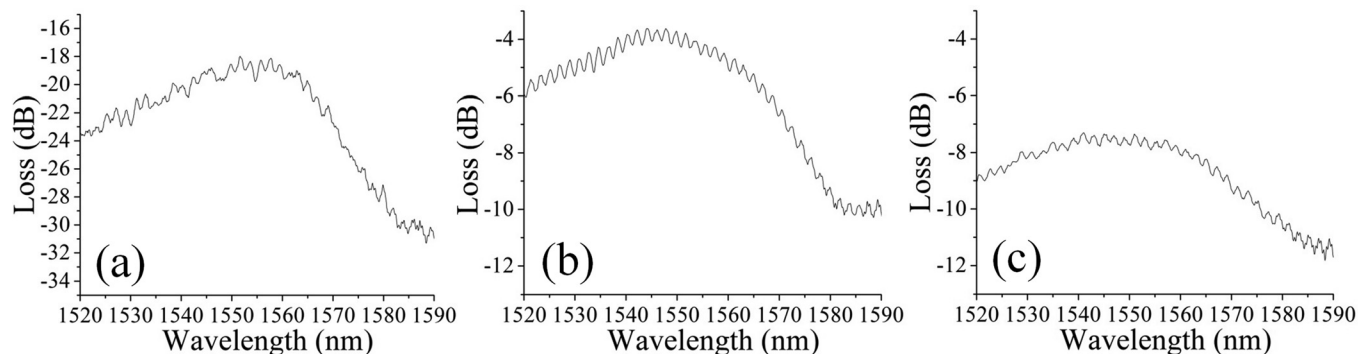


FIG. 5. (a) Measured coupling efficiency of all four gratings combined as shown in Fig. 1. (b) Measured coupling efficiency of grating 1. (c) Measured coupling efficiency of grating 4.

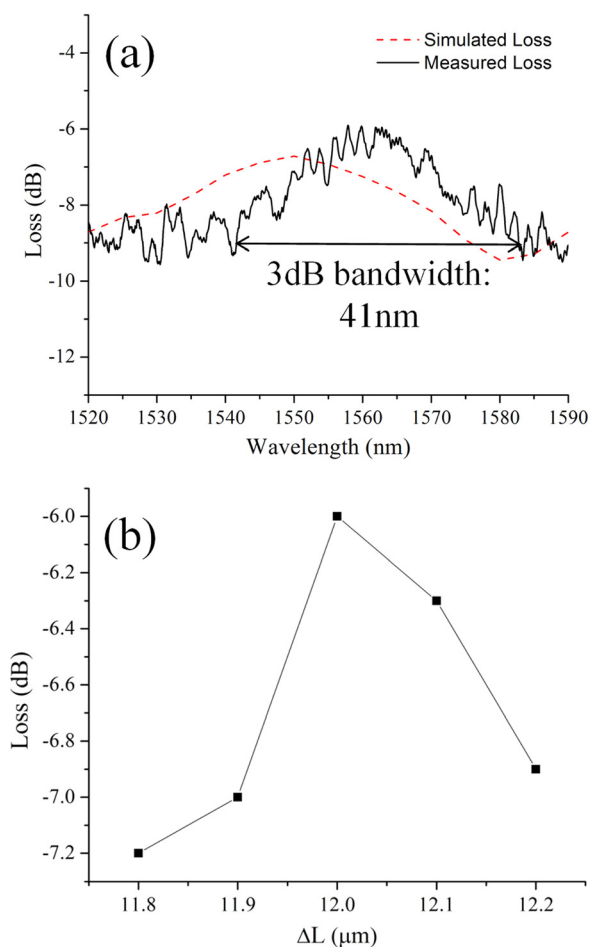


FIG. 6. (a) Simulated and measured coupling efficiencies of the inter-layer grating coupler. (b) Experimental inter-layer grating coupler efficiency at 1560 nm wavelength with different  $\Delta L$  value.

efficiency of all four gratings combined, as shown in Figure 6(a). The peak efficiency for the inter-layer grating coupler was measured to be 25% ( $-6.0$  dB) at 1560 nm wavelength with a 3 dB bandwidth of 41 nm. The simulated coupling efficiency is also shown in Figure 6(a). The peak wavelength shift is possibly due to fabrication errors. Comparing to the simulated result, the experimental result shows a higher peak efficiency but a lower bandwidth because of the local maxima and minima probably induced by reflections between the two silicon nanomembranes.<sup>16</sup> We experimentally varied  $\Delta L$  (as defined in Figures 1 and 2) over several samples and measured their coupling efficiencies at the target wavelength of 1560 nm. The efficiency drop is less than 1 dB when  $\Delta L = 12.0 \pm 0.1 \mu\text{m}$ , as shown in Figure 6(b), which means that the misalignment-induced efficiency drop can be controlled within 1 dB with the EBL system.

In conclusion, we presented a fabrication process flow to fabricate double-layer, on-chip, single crystalline silicon nanomembranes. We demonstrated simultaneous coupling to

separate photonic layers using subwavelength nanostructure based intra-chip grating couplers. The peak coupling efficiency to the bottom (top) layer is 18% (44%) at 1550 nm operating wavelength with TE polarization. We also demonstrated an on-chip subwavelength nanostructure based inter-layer grating coupler with a peak efficiency of 25% at 1560 nm operating wavelength with TE polarization and a 3 dB bandwidth of 41 nm. This approach serves as a platform for 3D photonic integration and 3D photonic devices, such as optical phased arrays (OPAs).<sup>23</sup>

This research was supported by the Multi-disciplinary University Research Initiative (MURI) program through the AFSOR (Contract No. FA 9550-08-1-0394).

- <sup>1</sup>R. Soref, *J. Sel. Top. Quantum Electron.* **12**, 1678 (2006).
- <sup>2</sup>M. Lipson, *J. Lightwave Technol.* **23**, 4222 (2005).
- <sup>3</sup>B. Anahui, D. Guckenberger, D. Kucharski, and A. Narasimha, *J. Solid-State Circuits* **41**, 2945 (2006).
- <sup>4</sup>W. Bogaerts, P. Dumon, D. V. Thourhout, and R. Baets, *Opt. Lett.* **32**, 2801 (2007).
- <sup>5</sup>D. Kwong, Y. Zhang, A. Hosseini, Y. Liu, and R. T. Chen, *Electron. Lett.* **46**, 1281 (2010).
- <sup>6</sup>M. J. Kobrinsky, B. A. Block, J.-F. Zheng, B. C. Barnett, E. Mohammed, M. Reshotko, F. Robertson, S. List, I. Young, and K. Cadien, *Intel Technol. J.* **8**, 129 (2004).
- <sup>7</sup>J. A. Kash, in *Conference on Photonics in Switching*, 19–22 August 2007, pp. 55–56.
- <sup>8</sup>J. Kang, Y. Atsumi, M. Oda, T. Amemiya, N. Nishiyama, and S. Arai, *Jpn. J. Appl. Phys.* **50**, 120208 (2011).
- <sup>9</sup>K. Preston, B. Schmidt, and M. Lipson, *Opt. Express* **15**, 17283 (2007).
- <sup>10</sup>J. Kang, Y. Atsumi, M. Oda, T. Amemiya, N. Nishiyama, and S. Arai, *Jpn. J. Appl. Phys.* **51**, 120203 (2012).
- <sup>11</sup>M. J. Zablocki, A. Sharkawy, O. Ebil, and D. W. Prather, *Opt. Lett.* **36**, 58 (2011).
- <sup>12</sup>Y. Zhang, A. Carlson, S. Y. Yang, A. Hosseini, D. Kwong, J. A. Rogers, and R. T. Chen, "Double-layer photonic devices based on transfer printing of silicon nanomembranes for three-dimensional photonics," in *Conference on Lasers and Electro-Optics, 6 May 2012* (OSA, 2012), paper CTu1A.
- <sup>13</sup>Y. Zhang, A. Hosseini, J. Ahn, D. Kwong, B. Fallahzad, E. Tutuc, and R. T. Chen, *Appl. Phys. Lett.* **100**, 181102 (2012).
- <sup>14</sup>X. Xu, H. Subbaraman, A. Hosseini, D. Kwong, and R. T. Chen, *Proc. SPIE* **8629**, 86291G (2013).
- <sup>15</sup>F. V. Laere, G. Roelkens, M. Ayre, J. Schrauwen, D. Tailaert, D. V. Thourhout, T. F. Krauss, and R. Baets, *J. Lightwave Technol.* **25**, 151 (2007).
- <sup>16</sup>S. Bernabe, C. Kopp, M. Volpert, J. Harduin, J. Fedeli, and H. Ribot, *Opt. Express* **20**, 7886 (2012).
- <sup>17</sup>J. Yao, X. Zheng, G. Li, I. Shubin, H. Thacker, Y. Luo, K. Raj, J. E. Cunningham, and A. V. Krishnamoorthy, in *2011 8th IEEE International Conference on Group IV Photonics*, 14–16 September 2011, pp. 383–385.
- <sup>18</sup>M. Cabezon, I. Garces, A. Villafranca, J. Pozo, P. Kumar, and A. Kazmierczak, *Appl. Opt.* **51**, 8090 (2012).
- <sup>19</sup>X. Xu, H. Subbaraman, J. Covey, D. Kwong, A. Hosseini, and R. T. Chen, *Appl. Phys. Lett.* **101**, 031109 (2012).
- <sup>20</sup>H. Subbaraman, X. Xu, J. Covey, and R. T. Chen, *Opt. Express* **20**, 20659 (2012).
- <sup>21</sup>X. Chen and H. K. Tsang, *Opt. Lett.* **36**, 796 (2011).
- <sup>22</sup>K. K. Tung, W. H. Wong, and E. Y. B. Pun, *Appl. Phys. A* **80**, 621 (2005).
- <sup>23</sup>A. Hosseini, D. Kwong, Y. Zhang, S. A. Chandorkar, F. Crnogorac, A. Carlson, B. Fallah, S. Bank, E. Tutuc, J. Rogers, R. F. W. Pease, and R. T. Chen, *J. Vac. Sci. Technol. B* **28**, C6O1 (2010).