0.88-THz Optical Clock Distribution on Adhesively Bonded Silicon Nanomembrane

Yang Zhang, Xiaochuan Xu, David Kwong, John Covey, Amir Hosseini, and Ray T. Chen

***Abstract*— Silicon photonics is a promising solution for on-chip optical clock distribution. We developed an adhesive bonding process to integrate silicon nanomembranes onto silicon chips. The single-mode strip waveguide fabricated on this adhesively bonded silicon membrane has a propagation loss of 4.3 dB/cm. A grating-coupled 1-to-32 H-tree optical distribution is experimentally demonstrated. Each branch includes 1.1-cm long strip waveguides, five Y-splitters, and three 90° bends. This optical distribution has a insertion loss of 13.9 dB, uniformity of 0.72 dB, and 3-dB bandwidth of 880 GHz determined by optical autocorrelation.**

***Index Terms*— Optical clock distribution, silicon nanomembrane, adhesive bonding.**

I. Introduction

OPTICAL interconnects offers potential benefits compared to conventional metallic interconnects in the continuing trend toward higher bandwidth in advanced VLSI circuits. Optics can deliver particularly precise timing of signals because of the low dispersion in optical channels, which is ideal for clock signal distribution [1]–[3]. Board-level and inter-chip optical clock distribution have been studied extensively [4]–[6]. On-chip optical clock distribution using an H-tree structure has been demonstrated on the silicon-on-insulator (SOI) platform [7], [8]. However, these demonstrations limit the optical clock distribution network and the electronic components to the same SOI substrate, which is not compatible with a typical CMOS bulk process. In order to maximize the design flexibility of an optical clock distribution network, it is preferable to stack photonic layers vertically on other electronic layers.

Back-end integration of photonics has been suggested to realize 3D integration of photonics on bulk silicon and has been demonstrated recently in [9] and [10], where deposited silicon nitride was used as a waveguiding material. Ultra-low loss silicon nitride waveguide can be fabricated by annealing and thermal cycling of low-pressure chemical vapor deposition (LPCVD) silicon nitride. However, this process is not compatible with the thermal budget of CMOS back-end processes. Plasma enhanced chemical vapor deposition (PECVD) is compatible with CMOS back-end process, but PECVD deposited silicon nitride waveguide shows 6 dB/cm propagation loss in the C-band due to Si-H and N-H bond absorption harmonics [11]. Moreover, silicon nitride lacks any mechanism for high-speed modulation, limiting it to either passive devices or slower devices using the thermo-optic (TO) effect.

Single-crystalline silicon offers the best set of optical and electrical properties for 3D integration of silicon photonics. In this letter, we present the experimental demonstration of a 1-to-32 H-tree optical distribution on a single-crystalline silicon nanomembrane. The silicon nanomembrane is adhesively bonded onto a silicon chip to serve as a platform for 3D integration of silicon photonics. By using the presented method, high-performance optical clock distribution networks can be vertically integrated onto existing electronic chips.

II. Device Design

The 1-to-32 optical distribution follows an H-tree geometry, in which the waveguide lengths, the number of 90° bends and splitters are identical for the input to each outputs of the optical distribution. Strip silicon waveguides with a cross-sectional dimension of 500 nm × 250 nm are used, which provide stronger light confinement compared to shallow etched rib waveguides. The H-tree geometry includes compact Y-splitters based on arc-shaped branching waveguides [12]. This kind of 1-to-2 splitter is not sensitive to refractive index variations due to temperature and/or thickness variations of silicon layers and also insensitive to unwanted residues and air voids in the junction region comparing to Y-splitters based on straight branching waveguides. The radii of the arcs are chosen to be 10 μm to avoid significant bending loss [13]. This value is also used in the 90° bends in the H-tree geometry.

A schematic of the designed 1-to-32 H-tree optical distribution is shown in Fig. 1. The 32 outputs cover an area of 4 mm × 4 mm. In order to perform optical characterization, subwavelength nanostructure based grating couplers described in [14] with 900 μm linear tapers are connected to all input and output waveguides to couple light in and out of the H-tree structure. All output waveguides are folded to align in one direction to simplify alignment between the grating couplers and optical fibers.

III. Device Fabrication

The process flow is shown in Fig. 2. Two SOI chips, which are both from a SOI wafer with a 250 nm thick silicon layer

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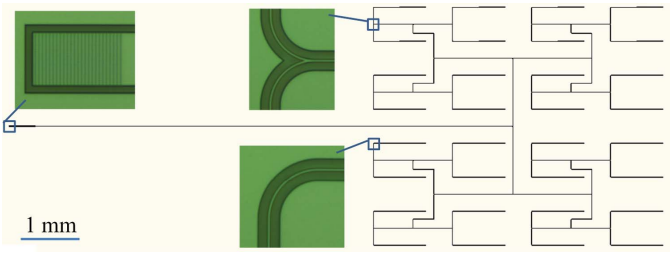

Fig. 1. Schematic of the H-tree optical distribution with 1.1 cm long strip waveguide, five Y-splitters, three 90° bends and two grating couplers with linear tapers. Optical microscope images of the grating coupler, Y-splitter and 90° bend are inserted.

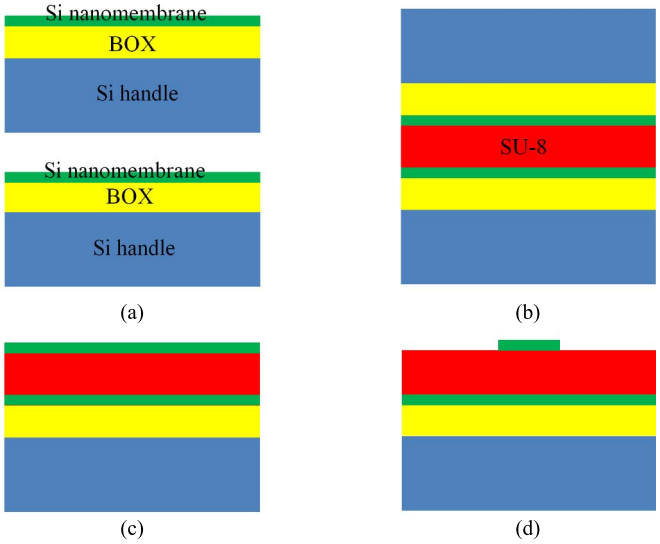

Fig. 2. Schematic of the fabrication process flow. (a) Substrates preparation. (b) Adhesive bonding. (c) Si handle and BOX removal. (d) Device fabrication.

and a 3 μm buried oxide (BOX) layer, were used in the adhesive bonding process, as shown in Fig. 2(a). ~1.5 μm thick SU-8 layers were spun onto both the SOI chips, followed by a 2 minute pre-bake at 95 °C to evaporate the solvent. Next, the two substrates were brought in close contact using a home-made chip bonder, which uniformly applied pressure and was kept in a 90 °C oven to ensure sufficient reflow of SU-8 for trapped air bubble removal to give a high quality bond (Fig. 2(b)).

The silicon handle of the top SOI chip was first mechanically polished to ~100 μm thick and then completely removed by deep reactive ion etching (DRIE). After DRIE, the top SOI chip without silicon handle became transparent to ultraviolet (UV) light. The sample was illuminated by 365 nm UV light through the top SOI chip to crosslink the SU-8 polymer. A post exposure bake at 65 °C was done to achieve a full crosslink of the SU-8. Once crosslinked, SU-8 has been proved to be very robust, which ensures the reliability of the clock distribution. After that, the BOX of the top SOI chip was removed by hydrofluoric acid wet etching, leaving a 250 nm thick silicon nanomembrane adhesively bonded to the bottom SOI chip for device fabrication, as shown in Fig. 2(c). When apply this technology on electronic chips, further investigation is required to verify the thermal compatibility and long term reliability.

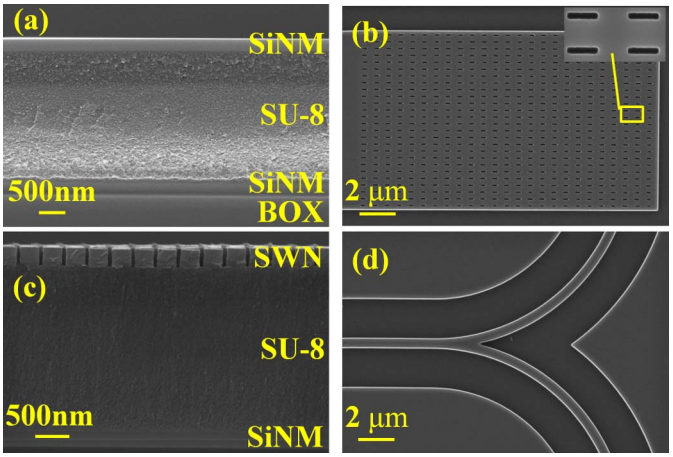

Fig. 3. SEM images of (a) cross section of a silicon nanomembrane adhesively bonded to a SOI substrate, (b) the grating coupler, (c) cross section of the subwavelength nanostructure, (d) the Y-splitter (SiNM denotes silicon nanomembrane, SWN denotes subwavelength nanostructure).

The adhesively bonded silicon nanomembrane can be patterned into the H-tree structure through electron beam (EB) lithography and etching steps, as shown in Fig 2(d). The waveguides were defined by exposing two 2 μm wide air trenches on each side of the waveguides using ZEP520A EB resist. The exposed sample was etched with HBr/Cl_2 based reactive ion etching (RIE). After etching, the sample was exposed to O_2 plasma in an RIE tool for 30s, followed by a bath in 90° remover PG, to remove the photoresist residue.

A cross-sectional scanning electron microscope (SEM) image of a silicon nanomembrane adhesively bonded to a SOI substrate is shown in Fig. 3(a). Top-down and cross-sectional SEM images of the subwavelength nanostructure based grating coupler are shown in Fig. 3(b) and (c). Fig. 3(d) shows the SEM image of the Y-splitter.

IV. Device Characterization

The propagation loss of 500 nm wide single-mode waveguides fabricated on the adhesively bonded silicon nanomembranes was first measured using the cut-back method. Serpentine patterns with the same number of bends but different waveguide lengths (10 mm, 20 mm, 30 mm, 40 mm and 50 mm) were fabricated. Subwavelength nanostructure based grating couplers were utilized for input and output light coupling. A polarization maintaining fiber (PMF) was used to couple transverse-electric (TE) polarized light at 1550 nm wavelength into the waveguides. The output light was collected by a single-mode fiber (SMF) and was measured by an optical power meter. The result is presented in Fig. 4. The propagation loss of the single-mode waveguide on the adhesively bonded silicon nanomembrane is 4.3 dB/cm at 1550 nm wavelength. This value is 1.2 dB/cm higher than that of single-mode waveguides fabricated on SOI wafers using the same processing equipment and recipes [15]. In order to investigate the source of this additional loss, the top surface roughness of the adhesively bonded silicon nanomembranes was measured using atomic force microscopy (AFM). The surface roughness of the adhesively bonded silicon nanomembrane

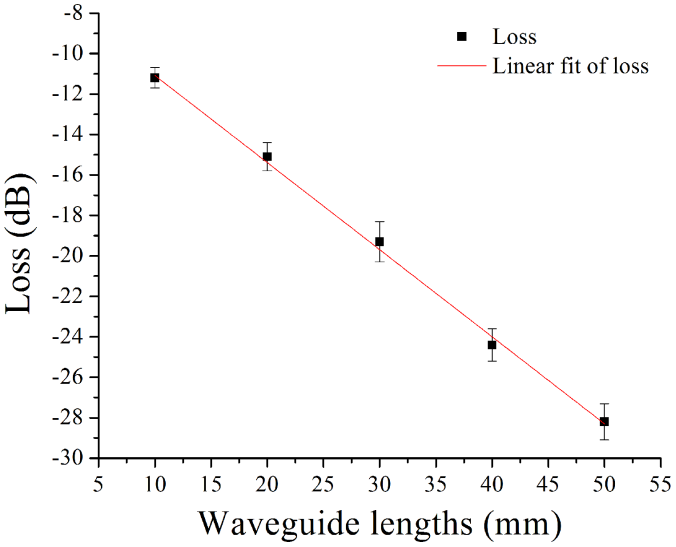

Fig. 4. Propagation loss of single-mode waveguide on adhesively bonded silicon nanomembrane determined by varying waveguide lengths using the cut-back method.

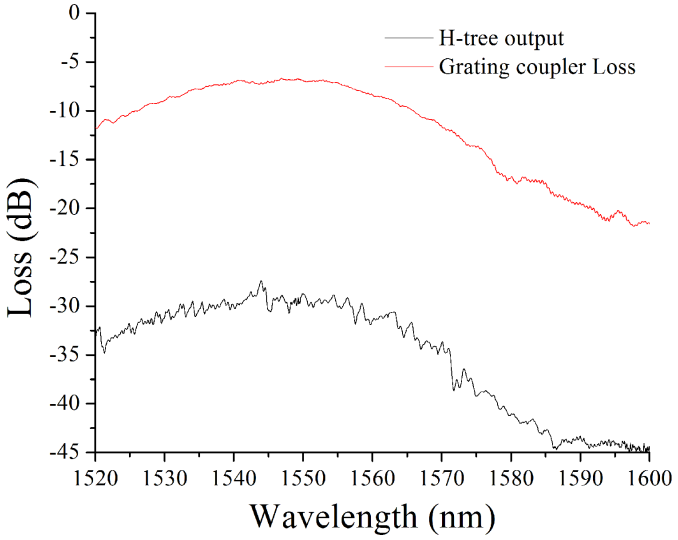

Fig. 5. Transmission spectra of the H-tree optical distribution (black) and the two grating couplers for input and output (red).

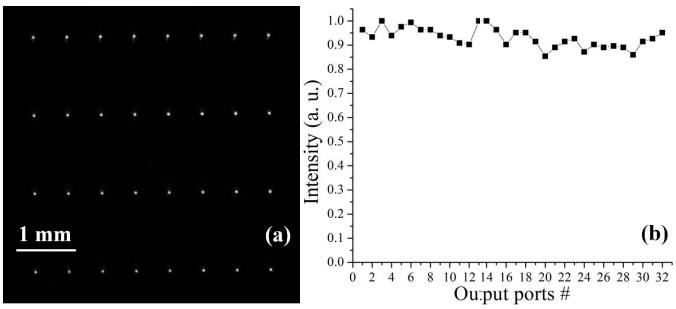

Fig. 6. (a) A top-down IR image of the 1-to-32 optical distribution, (b) measured intensities from each outputs of the H-tree structure.

was 0.629 nm, while it was 0.128 nm for SOI [15]. We conclude that the additional propagation loss is from the increased surface roughness of the adhesively bonded silicon nanomembrane. The propagation loss can be reduced by replacing our RIE with inductively coupled plasma (ICP) etching, which reduces the sidewall roughness of etched waveguides by lowering the required radio frequency (RF) bias voltage in etching [16].

In order to characterize the total excess loss of the H-tree optical distribution, TE polarized light was used as the input, and a power meter was used to detect the output power from each output at 1550 nm wavelength. The total excess loss, which excludes the fiber-to-waveguide coupling loss and the waveguide propagation loss, is defined as $-\log[(\sum I_m)/I_{in}]$, where I_m is the intensity of the m^{th} output channel, and I_{in} is the output intensity of a reference waveguide on the same chip with the same input and output grating couplers and waveguide length as the H-tree structure. The excess loss of the H-tree optical distribution at 1550 nm wavelength was measured to be 2.2 dB, which is mainly from the excess losses of five 1-to-2 Y-splitters. The average excess loss per Y-splitter is 0.44 dB, which is comparable to the results presented in [12].

The transmission spectrum of the H-tree optical distribution was also characterized. TE polarized light from a broadband amplified spontaneous emission (ASE) source was coupled to the H-tree structure through an input grating coupler, and the output light from one output of the H-tree structure was analyzed by an optical spectrum analyzer (OSA). The transmission spectrum obtained by normalizing the output signal to the light source has a peak value of −29 dB at around 1550 nm wavelength, as shown in Fig. 5. This −29 dB includes the device's insertion loss induced by grating couplers, Y-splitters, and waveguide, and the fanout loss of a 1-to-32 geometry. The two grating couplers' transmission spectrum was obtained by the method described in [17] and is shown in Fig. 5. The grating coupler has a peak efficiency of 45% (−3.5 dB) at 1550 nm operating wavelength. Considering the excess loss of five Y-splitters to be 2.2 dB, the waveguide propagation loss to be 4.7 dB (4.3 dB/cm × 1.1 cm), and the fanout loss to be 15 dB, the transmission spectrum agrees well with our previous loss characterizations. The transmission spectra of grating couplers and H-tree optical distribution have similar profiles through an 80 nm bandwidth, meaning the Y-splitters and waveguide have nearly constant loss in this wide bandwidth.

A top-down infrared (IR) image of the entire optical distribution is shown in Fig. 6(a). At each output of the optical distribution, TE polarized light at 1550 nm wavelength was coupled out from the grating coupler, and the near field image was collected by an IR CCD camera suspended above the grating coupler. The observation clearly shows 32 outputs. Quantitative measurements of the intensities from each output were performed to characterize the uniformity of this H-tree optical distribution, as shown in Fig. 5(b). The uniformity, which is defined as $10\log(I_{max}/I_{min})$, is calculated to be 0.72 dB.

The bandwidth of the H-tree optical distribution was characterized by optical autocorrelation as described in [18]. In order to obtain enough optical signal for autocorrelation, a testing waveguide, which has the exact geometry and dimensions as one arm of the H-tree structure (including input & output grating couplers with linear tapers, 1.1cm single-mode waveguide, and eight 90° bends), was used. A TE polarized optical pulse generated from a femtosecond laser with a center wavelength

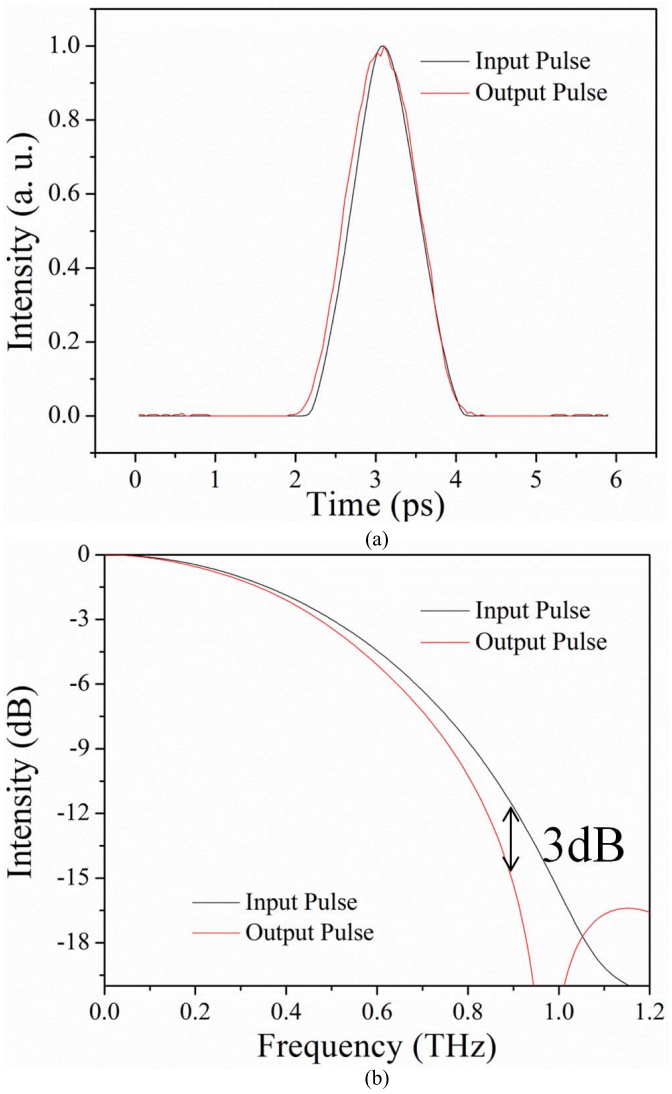

Fig. 7. (a) Input and output pulses in the time domain, (b) input and output pulses in the frequency domain.

of 1550 nm was launched into the testing waveguide through a PMF. The output signal was collected by a SMF, amplified by an erbium doped fiber amplifier (EDFA), and finally fed into an autocorrelator. The input and output optical pulses in time domain are shown in Fig. 7(a). The intensity of the output pulse is normalized to the intensity of the input pulse. The output pulse is broadened in the time domain after going through the testing waveguide. The frequency domain responsivity of the input and output pulses, obtained by the fast Fourier transform of the pulses in time domain, are shown in Fig. 7(b). The 3 dB bandwidth of the device is found to be 880 GHz. The bandwidth limiting factor is not the dispersion of the single-mode waveguide, but the optical nonlinearities induced by the high peak power of the femtosecond pulse [19], and the dispersion of the grating couplers. The bandwidth could be larger because the average power of an optical link is much lower than the peak power of the femtosecond pulse.

V. Conclusion

In summary, a 1-to-32 H-tree optical distribution network was fabricated on adhesively bonded silicon nanomembrane. The single-mode waveguides fabricated on this platform has a propagation loss of 4.3 dB/cm. The H-tree structure has a insertion loss of 13.9 dB and an output uniformity of 0.72 dB. This grating-coupled H-tree structure has a 3 dB bandwidth of 880 GHz measured by autocorrelation, which is sufficient to support the interconnect bandwidth requirement in future VLSI chips.

References

[1] R. T. Chen *et al.*, "Fully embedded board-level guided-wave optoelectronic interconnects," *Proc. IEEE*, vol. 88, no. 6, pp. 780–793, Jun. 2000.
[2] D. A. B. Miller, "Optical interconnects to electronic chips," *Appl. Opt.*, vol. 49, no. 25, pp. F59–F70, 2010.
[3] C. Thangaraj, R. Pownall, P. Nikkel, G. Yuan, K. L. Lear, and T. Chen, "Fully CMOS-compatible on-chip optical clock distribution and recovery," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 10, pp. 1385–1398, Oct. 2010.
[4] R. T. Chen, F. Li, M. Dubinovsky, and O. Ershov, "Si-based surface-relief polygonal gratings for 1-to-many wafer scale optical clock signal distribution," *IEEE Photon. Technol. Lett.*, vol. 8, no. 8, pp. 1038–1040, Aug. 1996.
[5] C. Zhao and R. T. Chen, "Performance consideration of three-dimensional optoelectronic interconnection for intra-multichip-module clock signal distribution," *Appl. Opt.*, vol. 36, no. 12, pp. 2537–2544, 1997.
[6] J. Gan, L. Wu, H. Luan, B. Bihari, and R. T. Chen, "Two-dimensional 45° surface-normal microcoupler array for guided-wave optical clock distribution," *IEEE Photon. Technol. Lett.*, vol. 11, no. 11, pp. 1452–1454, Nov. 1999.
[7] T. Fukazawa, A. Sakai, and T. Baba, "H-tree-type optical clock signal distribution circuit using a Si photonic wire waveguide," *Jpn. J. Appl. Phys.*, vol. 41, no. 12B, pp. L1461–L1463, 2002.
[8] L. Vivien *et al.*, "Experimental demonstration of a low-loss optical H-tree distribution using silicon-on-insulator microwaveguide," *Appl. Phys. Lett.*, vol. 85, no. 5, pp. 701–703, 2004.
[9] A. Biberman and K. Bergman, "Optical interconnection networks for high-performance computing systems," *Rep. Prog. Phys.*, vol. 75, no. 4, p. 046402, 2012.
[10] Y. H. D. Lee and M. Lipson, "Back-end deposited silicon photonics for monolithic integration on CMOS," *IEEE J. Sel. Topics Quantum Electron.*, vol. 19, no. 2, Mar./Apr. 2013, Art. ID 8200207.
[11] N. Sherwood-Droz and M. Lipson, "Scalable 3D dense integration of photonics on bulk silicon," *Opt. Exp.*, vol. 19, no. 18, pp. 17758–17765, 2011.
[12] S. H. Tao, Q. Fang, J. F. Song, M. B. Yu, G. Q. Lo, and D. L. Kwong, "Cascade wide-angle Y-junction 1×16 optical power splitter based on silicon wire waveguides on silicon-on-insulator," *Opt. Exp.*, vol. 16, no. 26, pp. 21456–21461, Dec. 2008.
[13] Y. A. Vlasov and S. J. McNab, "Losses in single-mode silicon-on-insulator strip waveguides and bends," *Opt. Exp.*, vol. 12, no. 8, pp. 1622–1631, 2004.
[14] Y. Zhang *et al.*, "On-chip intra- and inter-layer grating couplers for three-dimensional integration of silicon photonics," *Appl. Phys. Lett.*, vol. 102, no. 21, p. 211109, 2013.
[15] X. Xu, H. Subbaraman, D. Kwong, A. Hosseini, Y. Zhang, and R. T. Chen, "Large area silicon nanomembrane photonic devices on unconventional substrates," *IEEE Photon. Technol. Lett.*, vol. 25, no. 16, pp. 1601–1604, Aug. 15, 2013.
[16] J. H. Kang, Y. Atsumi, M. Oda, T. Amemiya, N. Nishiyama, and S. Arai, "Low-loss amorphous silicon multilayer waveguides vertically stacked on silicon-on-insulator substrate," *Jpn. J. Appl. Phys.*, vol. 50, no. 12R, p. 120208, 2011.
[17] X. Xu, H. Subbaraman, J. Covey, D. Kwong, A. Hosseini, and R. T. Chen, "Complementary metal–oxide–semiconductor compatible high efficiency subwavelength grating couplers for silicon integrated photonics," *Appl. Phys. Lett.*, vol. 101, no. 3, pp. 031109-1–031109-4, Jul. 2012.
[18] X. Wang, L. Wang, W. Jiang, and R. T. Chen, "Hard-molded 51 cm long waveguide array with a 150 GHz bandwidth for board-level optical interconnects," *Opt. Lett.*, vol. 32, no. 6, pp. 677–679, 2007.
[19] E. Dulkeith, F. Xia, L. Schares, W. M. J. Green, and Y. A. Vlasov, "Group index and group velocity dispersion in silicon-on-insulator photonic wires," *Opt. Exp.*, vol. 14, no. 9, pp. 3853–3863, 2006.